REMARKS

The Office Action mailed December 1, 2004 has been received and the Examiner's comments carefully reviewed. Prior to entry of this paper, Claims 1-4, 6-15, and 17-20 were pending. Claims 1-4, 6-15, and 17-20 were rejected. In this paper, Claims 1, 9, and 10 were amended to further clarify the subject matter Applicant regards as his invention. Claims 1-4, 6-15, and 17-20 are currently pending. No new subject matter has been added. For at least the following reasons, Applicant respectfully submits that each of the presently pending claims is in condition for allowance.

Claim Rejections

Claims 1-3, 6, 7, and 9-15 were rejected under 35 U.S.C. § 102(b) as being anticipated by Razavi. Claim 4, 8, and 17-20 were rejected under 35 U.S.C § 103(a) as being unpatentable over Razavi in view of Sudjian.

It is respectfully submitted that Claims 1, 9, and 10 are allowable at least because Razavi does not disclose "the modulus control signal is ignored at least until after the onset of a next input pulse is received", as recited in Applicant's Claims 1, 9, and 10.

In contrast, Razavi describes a pulse-swallow divider that is illustrated in Fig. 8.28. "The divider consists of a prescaler, a program counter, and a swallow counter." (Page 270, paragraph 2 of Razavi) Also, "(1) the prescaler divides the input by either N+1 or N according to the logical state of the modulus control line, (2) the program counter always divides the prescaler output by P, and (3) the swallow counter divides the prescaler output by S." (Page 270, paragraph 2 of Razavi).

Each time the swallow counter is reset, the swallow counter changes the status of the modular control line to make the prescaler divide the input signal by N+1. (See page 270, paragraph 3 of Razavi). The prescaler continues to divide by (N+1) for (N+1)*S cycles of the input signal. (See page 270, paragraph 3 of Razavi). Then, when (N+1)*S cycles of the input signal have occurred since the swallow counter was last reset, the swallow counter changes the state of the modulus control line, making the prescaler divide by N rather than N+1. (See page 270, paragraph 3 of Razavi). Then, after another [(P-S)*N] pulses of the input signal, or [P*N + S] cycles of the

input signal since the swallow counter was last reset, the swallow counter is reset. (See page 270, paragraph 3 of Razavi). At this point, the swallow counter changes the status of the modulus control line so that the prescaler divides by N+1 again, repeating the operation. (See page 270, paragraph 3 of Razavi).

For the pulse-swallow divider described in Razavi, when [P*N]+S cycles have occurred after the last time the swallow counter was reset, the swallow counter changes the status of the modulus control line so that the prescaler divides by N+1. (See page 270, paragraph 3 of Razavi). Accordingly, at the onset of the next clock cycle, the prescaler is dividing the input signal by N+1 instead of N. (See page 270, paragraph 3 of Razavi). Razavi does NOT disclose ignoring the modulus control signal.

In contrast, Applicant's Claims 1, 9, and 10 recite "the modulus control signal is ignored at least until after the onset of a next input pulse is received."

For at least the reasons stated above, it is respectfully submitted that Claims 1, 9, and 10 are allowable, and notice to that effect is respectfully requested.

In order to further aid the reader's understanding, one embodiment of Applicant's invention is discussed in this paragraph. This embodiment is described by way of example only, and therefore shall not be construed as limiting, and shall not give rise to any type of estoppel whatsoever. One non-limiting embodiment of the invention may be understood more clearly with reference to Applicant's FIGURE 9. As shown in Applicant's FIGURE 9, a period of time, CPD9 962, occurs from the M^{th} pulse of signal clkin(faster) to the falling edge of modulus control signal DIV4, where M=[P*N+S]. As shown in the figure, time CPD9 962 is sufficiently large that the next pulse (i.e. the $(M+1)^{th}$ pulse) of signal clkin(faster) occurs prior to the falling edge of modulus control signal DIV4. However, the prescaler ignores modulus control signal DIV4 at the onset of the $(M+1)^{th}$ pulse of signal clkin(faster) (see page 8, lines 27-30 of Applicant's specification as filed). Accordingly, in this embodiment, the fact that time CPD9 962 has not elapsed by the onset of the $(M+1)^{th}$ pulse is irrelevant. **Because the modulus control signal is ignored by the prescaler** until after the onset of the next pulse after the M^{th} pulse (where the M^{th} pulse is the $[P*N+S]^{th}$ pulse), the

period of input signal clkin may be less than period of time CPD9 962 (which is the period of time from the $[P*N+S]^{th}$ pulse of input signal clkin to the falling edge of modulus control signal DIV4).

In contrast, for the pulse-swallow divider described in Razavi, the period of the input signal must be greater that the period of time from the beginning of the $[P*N+S]^{th}$ pulse of the input signal to the falling edge of the modulus control signal.

Claims 2-8 are respectfully submitted to be allowable at least because they depend on Claim 1, which is proposed to be allowable. Claim 11-20 are respectfully submitted to be allowable at least because they depend on Claim 10, which is proposed to be allowable.

Inadvertent omission in Claim 20

Applicant filed an amendment on July 15, 2004 in which, inter alia, Claim 20 was amended. In the amendment filed on July 15, 2004, Claim 20 was amended to change the claim dependency from Claim 16 to Claim 10. In the original Claim 20, Claim 20 spanned 9 lines (Claim 20, lines 1-9). However, in the amendment filed on July 15, 2004, the portion of Claim 20 from lines 5-9 was inadvertently omitted.

In this paper, Claim 20 has been presented with the material from the original Claim 20 that was inadvertently omitted in the amendment filed on July 15, 2004. Including the portion of the original Claim 20 that was inadvertently omitted in the amendment filed on July 15, 2004, was not treated as an amendment to Claim 20 in this paper, because the inadvertently omitted material was (obviously) not marked as a deletion in the amendment filed on July 15, 2004.

Conclusion

It is respectfully submitted that each of the presently pending claims (1-4, 6-15, and 17-20) are in condition for allowance and notification to that effect is requested. The Examiner is invited to contact Applicant's representative at the below-listed telephone number if it is believed that prosecution of this application may be assisted thereby. Although certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentably distinct. Applicant reserves the right to raise these arguments in the future.

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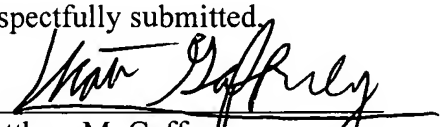
Respectfully submitted,

By 

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